ABSTRACT

The present invention provides a method for parallel production of an MOS transistor in an MOS area of a substrate and a bipolar transistor in a bipolar area of the substrate. The method comprises generating an MOS preparation structure in the MOS area, wherein the MOS preparation structure comprises an area provided for a channel, a gate dielectric, a gate electrode layer and a mask layer on the gate electrode layer. Further, a bipolar preparation structure is generated in the bipolar area, which comprises a conductive layer and a mask layer on the conductive layer. The mask layer is thinned in the area of the gate electrode. For determining a gate electrode and a base terminal area, common structuring of the gate electrode layer and the conductive layer is performed.
Figure 26